

IN THE FIGURES:

Please replace Figures 16-21 with the attached replacement sheets. The Figures 16-21 are labeled as "PRIOR ART".

REMARKS:

Applicants are submitting this Amendment and Response in reply to the Official Action dated March 28, 2007 and Applicants believe that the Amendment and Response is fully responsive to the Official Action for at least the reasons set forth herein.

Applicants would like to thank the Examiner for indicating that Claims 2 and 4-13 have allowable subject matter and would be allowed if rewritten in independent form including all of the limitations of the rejected base claim and any intervening claims.

In the outstanding Official Action, Claims 1 and 3 stand rejected under 35 U.S.C. § 103 (a) as being unpatentable over Applicants Admitted Prior Art (AAPA) in view of Joo, U.S. Patent No. 6,762,970.

Applicants respectfully disagree with the rejection and traverse with at least the following analysis.

Applicants submit that the cited combination fails to teach or suggest all of the limitations of Claims 1 and 3. Specifically, the reference fails to disclose a boost circuit for charging parasitic capacitors by a time when an amount of a current flowed by said constant current source reaches an amount of a current required to write information into the storage element at a predetermined position related to the storage element, as recited in Claim 1, and that the boost circuit comprises a condenser for storing charge to charge the parasitic capacitors, as recited in Claim 3.

While Joo appears to disclose a boost circuit, the boost circuit is used for **reading** and not writing. In Joo, Figure 1 illustrates a flash memory device using a boosting circuit for reading out a conventional flash memory.

Additionally, Joo teaches away from using the claimed boost circuit. The reference describes that loading from the boost circuit to the word line is significantly large and, therefore, requires that the size of the capacitor of the boosting circuit be significantly large. This results in a substantial amount of time to boost the pumping capacitor up to a desired voltage. The **boosting circuit results in a problem in the speed of the read out.** See Col. 1, lines 49-59.

The very purpose of the invention in Joo was to **avoid using a boosting circuit** for the read-out. “Another objection of the present invention is to provide a flash memory device in which a word line is not boosted in a read-out mode and a boosting voltage is generated in a standby mode and a read-out mode, thus improving the read-out speed.” See Col. 1, line 64-Col. 2 line 2.

Pro arguendo, even if the reference did not teach away from using a boosting circuit and even if the reference did not teach that the boosting circuit is used in reading, the Examiner’s statement that the “pumping circuit” is the claimed boost circuit is incorrect. The two circuits are structurally different and the manner in which the circuit achieves its end result is different.

The claimed boost circuit stores electric charge at the time of write standby and instantaneously releases the electric charges at the time of write operation allowing for the parasitic capacitors to be instantaneously charged. The boost circuit includes a plurality of boost capacitors and a capacitor selector. As described in the specification when the write signal (WENX) and standby (VBSTX) are switched, the Pmos transistor (MBX) turns off and the Pmos transistor (MSX) turns on. The potential (VBX) will approximately equal the power supply voltage. Therefore, a charge stored on the boost

capacitor abruptly flows through the selected wire, charging the parasitic capacitors. See Figure 1 and page 15. Specifically, the boosting circuit of the claimed invention is designed to charge the parasitic capacitance rapidly.

In contrast, the pumping circuit does not “store electric current”. In fact, there is no storage element in the pumping circuit, e.g., condenser. The reference teaches away from using a condenser or capacitor. Crev is not part of the pumping circuit. The pumping circuit increases the output voltage at a specific time. The pumping voltage charges Crev. The pumping circuit pumps a voltage (not current). The reference is not even concerned with current.

Additionally, the reference does not teach a current source circuit, as recited in Claim 1. The reference describes that the voltage of the word line becomes higher than the voltage of the power source. The object of the cited reference is to obtain a desired voltage and improve the operations margin in the IC.

Accordingly, the claimed invention has an advantage over the prior art; the time it takes until the charging current reaches a desired value is shortened as a result of charging the parasitic capacitance.

Both the structure and the function of the claimed invention are fundamentally different than the prior art.

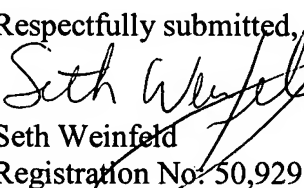
Therefore, the reference fails to teach, suggest or render obvious each and every limitation of Claims 1 and 3; the claims are patentable over the cited reference.

Furthermore, Applicants note that the Abstract has been amended herewith. The amendment obviates the Examiner’s objection.

Lastly, Applicants note that Figures 16-21 have been labeled as "Prior Art". Applicants submit replacement sheets herewith. Applicants believe that the replacement sheets obviate the objections to the figures.

Based upon the foregoing, Applicants respectfully request that the Examiner withdraw the rejection of Claims 1 and 3 pursuant to 35 U.S.C. § 103 (a). Additionally, Applicants respectfully request that the Examiner withdraw the objections to the figures and Abstract.

In conclusion, the Applicants believe that the above-identified application is in condition for allowance and henceforth respectfully solicits the Examiner to allow the application. If the Examiner believes a telephone conference might expedite the allowance of this application, the Applicants respectfully request that the Examiner call the undersigned, Applicants' attorneys, at the following telephone number: (516) 742-4343.

Respectfully submitted,

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Enclosures